## CLAIMS

We claim:

1. A method of forming a high $f_{MAX}$ deep submicron MOSFET; comprising the steps of:

providing a substrate having a MOSFET formed thereon; the MOSFET having a source and a drain and including a silicide portion over a gate electrode;

forming a first ILD layer over the substrate and the MOSFET;

planarizing the first ILD layer to expose the silicide portion over the gate electrode;

forming a metal gate portion over the planarized first ILD layer and over the silicide portion over the gate electrode; the metal gate portion having a width substantially greater than the width of the silicide portion over the gate electrode;

forming a second ILD layer over the metal gate portion and the first ILD layer;

forming a first metal contact through the second ILD layer contacting the metal gate portion and a second metal contact through the second and first ILD layers contacting the drain completing the formation of the high $f_{MAX}$ deep submicron MOSFET;

whereby the width of the metal gate portion reduces $R_g$ and increases the $f_{MAX}$ of the high $f_{MAX}$ deep submicron MOSFET.

2. The method of claim 1, including the step of forming a dielectric layer over the substrate and MOSFET before formation of the first ILD layer, and wherein the dielectric layer is removed over the silicide portion over the gate electrode before formation of the metal gate portion; and wherein the first ILD layer is planarized by a chemical-mechanical polishing process.

3. The method of claim 1, including the step of forming a dielectric layer comprised of $Si_3N_4$ or SiON over the substrate and MOSFET before formation of the first ILD layer, and wherein the dielectric layer is removed over the silicide portion over the gate electrode before formation of the metal gate portion; and wherein the first ILD layer is planarized by a chemical-mechanical polishing process.

4. The method of claim 1, wherein the gate electrode is comprised polysilicon; the silicide portion over the gate electrode is comprised of a material selected from the group consisting of $CoSi_x$, $CoSi_2$, and $TiSi_2$; the first ILD layer is comprised of a material selected from the group consisting of oxide, silicon oxide, USG and TEOS; the metal gate portion is comprised of a material selected from the group consisting of W, Al, Cu, TiN and Au; the second ILD layer is comprised of a material selected from the group consisting of oxide, silicon oxide, HDP and FSG; and the first and second metal contacts each comprised of a material selected from the group consisting of W and Cu.

5. The method of claim 1, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised $CoSi_x$; the first ILD layer is

comprised of silicon oxide; the metal gate portion is comprised of tungsten; the second ILD layer is comprised silicon oxide; and the first and second metal contacts each being comprised of tungsten.

6. The method of claim 1, wherein the gate electrode has a width of from about 500 to 5000Å and the metal gate portion has a width of from about 500 to 8000Å.

7. The method of claim 1, wherein the gate electrode has a width of from about 1000 to 3500Å and the metal gate portion has a width of from about 1000 to 3000Å.

8. The method of claim 1, wherein the gate electrode has a width of about 0.13μm and the metal gate portion has a width of from about 1800 to 2400Å.

9. The method of claim 1, wherein the gate electrode has a height of from about 1000 to 3000Å; the silicide portion over the gate electrode has a thickness of from about 270 to 330Å; the planarized first ILD layer has a thickness of from about 1700 to 1900Å; and the metal gate portion has a thickness of from about 1800 to 2200Å.

10. The method of claim 1, wherein the gate electrode has a height of from about 1500 to 2200Å; the silicide portion over the gate electrode has a thickness of from about 290 to 310Å; the planarized first ILD layer has a thickness of about 1800Å; and the metal gate portion has a thickness of from about 1900 to 2100Å.

11. The method of claim 1, wherein the gate electrode has a height of from about 1500 to 2200Å; the silicide portion over the gate electrode has a thickness of about 300Å; the planarized first ILD layer has a thickness of about 1800Å; and the metal gate portion has a thickness of about 2000Å.

12. The method of claim 1, wherein the MOSFET includes a source silicide portion over at least a portion of the source and a drain silicide portion over at least a portion of the drain; and wherein the second metal contact contacts the drain silicide portion.

13. The method of claim 1, wherein the MOSFET includes a source $CoSi_x$ silicide portion over at least a portion of the source and a drain $CoSi_x$ silicide portion over at least a portion of the drain; and wherein the second metal contact contacts the drain $CoSi_x$ silicide portion.

14. The method of claim 1, wherein the first ILD layer is planarized by a chemical-mechanical polishing process.

15. The method of claim 1, wherein the high $f_{MAX}$ deep submicron MOSFET is used in an RF circuit.

16. The method of claim 1, wherein the gate electrode has a gate oxide thereunder; the gate oxide having a thickness proximate the source and drain to significantly

reduce the parasitic capacitance and increase the $f_{max}$ of the high $f_{MAX}$ deep submicron MOSFET.

17. A method of forming a high $f_{MAX}$ deep submicron MOSFET, comprising the steps of:

providing a substrate 10 having a MOSFET formed thereon; the MOSFET having a source and a drain and including a silicide portion over a gate electrode; the gate electrode having a width of from about 500 to 5000Å;

forming a first ILD layer over the substrate and the MOSFET;

chemical-mechanically polishing the first ILD layer to expose the silicide portion over the gate electrode;

forming a metal gate portion over the planarized first ILD layer and over the silicide portion over the gate electrode 18; the metal gate portion having a width of from about 500 to 8000Å;

forming a second ILD layer over the metal gate portion and the first ILD layer;

forming a first metal contact through the second ILD layer contacting the metal gate portion and a second metal contact through the second and first ILD layers contacting the drain completing the formation of the high $f_{MAX}$ deep submicron MOSFET;

whereby the width of the metal gate portion reduces $R_g$ and increases the $f_{MAX}$ of the high $f_{MAX}$ deep submicron MOSFET.

18. The method of claim 17, including the step of forming a dielectric layer over the substrate and MOSFET before formation of the first ILD layer, and wherein the dielectric layer is removed over the silicide portion over the gate electrode before formation of the metal gate portion.

19. The method of claim 17, including the step of forming a dielectric layer comprised of $Si_3N_4$ or SiON over the substrate and MOSFET before formation of the first ILD layer, and wherein the dielectric layer is removed over the silicide portion over the gate electrode before formation of the metal gate portion.

20. The method of claim 17, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised of a material selected from the group consisting of $CoSi_x$, $CoSi_2$ and $TiSi_2$; the first ILD layer is comprised of a material selected from the group consisting of oxide, silicon oxide, USG and TEOS; the metal gate portion is comprised of a material selected from the group consisting of W, Al, Cu, TiN and Au; the second ILD layer is comprised of a material selected from the group consisting of oxide, silicon oxide, HDP and FSG; and the first and second metal contacts each comprised of a material selected from the group consisting of W and Cu.

21. The method of claim 17, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised $CoSi_x$; the first ILD layer is comprised of silicon oxide; the metal gate portion is comprised of tungsten; the

second ILD layer is comprised silicon oxide; and the first and second metal contacts each being comprised of tungsten.

22. The method of claim 17, wherein the gate electrode has a width of from about 1000 to 3500Å and the metal gate portion has a width of from about 1000 to 3000Å.

23. The method of claim 17, wherein the gate electrode has a width of about 0.13μm and the metal gate portion has a width of from about 1800 to 2400Å.

24. The method of claim 17, wherein the gate electrode has a height of from about 1000 to 3000Å; the silicide portion over the gate electrode has a thickness of from about 270 to 330Å; the planarized first ILD layer has a thickness of from about 1700 to 1900Å; and the metal gate portion has a thickness of from about 1800 to 2200Å.

25. The method of claim 17, wherein the gate electrode has a height of from about 1500 to 2200Å; the silicide portion over the gate electrode has a thickness of from about 290 to 310Å; the planarized first ILD layer has a thickness of about 1800Å; and the metal gate portion has a thickness of from about 1900 to 2100Å.

26. The method of claim 17, wherein the gate electrode has a height of from about 1500 to 2200Å; the silicide portion 30 over the gate electrode 18 has a thickness of about 300Å; the planarized first ILD layer has a thickness of about 1800Å; and the metal gate portion has a thickness of about 2000Å.

27. The method of claim 17, wherein the MOSFET includes a source silicide portion over at least a portion of the source and a drain silicide portion over at least a portion of the drain; and wherein the second metal contact contacts the drain silicide portion.

28. The method of claim 17, wherein the MOSFET includes a source $CoSi_x$ silicide portion over at least a portion of the source and a drain $CoSi_x$ silicide portion over at least a portion of the drain; and wherein the second metal contact contacts the drain $CoSi_x$ silicide portion.

29.The method of claim 17, wherein the high $f_{MAX}$ deep submicron MOSFET is used in an RF circuit.

30. The method of claim 17, wherein the gate electrode has a gate oxide thereunder; the gate oxide having a thickness proximate the source and drain to significantly reduce the parasitic capacitance and increase the $f_{max}$ of the high $f_{MAX}$ deep submicron MOSFET.

31. A method of forming a high $f_{MAX}$ deep submicron MOSFET, comprising the steps of:

providing a substrate having a MOSFET formed thereon; the MOSFET having a source and a drain and including a silicide portion over a gate electrode; the gate electrode having a gate oxide thereunder; the gate oxide having a

thickness proximate the source and drain to significantly reduce the parasitic capacitance and increase the $f_{max}$ of the high $f_{MAX}$ deep submicron MOSFET;

forming a first ILD layer over the substrate and the MOSFET;

planarizing the first ILD layer to expose the silicide portion over the gate electrode;

forming a metal gate portion over the planarized first ILD layer and over the silicide portion over the gate electrode; the metal gate portion having a width substantially greater than the width of the silicide portion over the gate electrode;

forming a second ILD layer over the metal gate portion and the first ILD layer;

forming a first metal contact through the second ILD layer contacting the metal gate portion and a second metal contact through the second and first ILD layers contacting the drain completing the formation of the high $f_{MAX}$ deep submicron MOSFET;

whereby the width of the metal gate portion reduces $R_g$ and increases the $f_{MAX}$ of the high $f_{MAX}$ deep submicron MOSFET.

32. The method of claim 31, including the step of forming a dielectric layer over the substrate and MOSFET before formation of the first ILD layer, and wherein the dielectric layer is removed over the silicide portion over the gate electrode before formation of the metal gate portion; and wherein the first ILD layer is planarized by a chemical-mechanical polishing process.

33. The method of claim 31, including the step of forming a dielectric layer comprised of $Si_3N_4$ or SiON over the substrate and MOSFET before formation of the first ILD layer, and wherein the dielectric layer is removed over the silicide portion over the gate electrode before formation of the metal gate portion; and wherein the first ILD layer is planarized by a chemical-mechanical polishing process.

34. The method of claim 31, wherein the gate electrode is comprised polysilicon; the silicide portion over the gate electrode is comprised of a material selected from the group consisting of $CoSi_x$, $CoSi_2$, and $TiSi_2$; the first ILD layer is comprised of a material selected from the group consisting of oxide, silicon oxide, USG and TEOS; the metal gate portion is comprised of a material selected from the group consisting of W, Al, Cu, TiN and Au; the second ILD layer is comprised of a material selected from the group consisting of oxide, silicon oxide, HDP and FSG; and the first and second metal contacts each comprised of a material selected from the group consisting of W and Cu.

35. The method of claim 31, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised $CoSi_x$; the first ILD layer is comprised of silicon oxide; the metal gate portion is comprised of tungsten; the second ILD layer is comprised silicon oxide; and the first and second metal contacts each being comprised of tungsten.

36. The method of claim 31, wherein the gate electrode has a width of from about 500 to 5000Å and the metal gate portion has a width of from about 500 to 8000Å.

37. The method of claim 31, wherein the gate electrode has a width of from about 1000 to 3500Å and the metal gate portion has a width of from about 1000 to 3000Å.

38. The method of claim 31, wherein the gate electrode has a width of about 0.13µm and the metal gate portion has a width of from about 1800 to 2400Å.

39. The method of claim 31, wherein the gate electrode has a height of from about 1000 to 3000Å; the silicide portion over the gate electrode has a thickness of from about 270 to 330Å; the planarized first ILD layer has a thickness of from about 1700 to 1900Å; and the metal gate portion has a thickness of from about 1800 to 2200Å.

40. The method of claim 31, wherein the gate electrode has a height of from about 1500 to 2200Å; the silicide portion over the gate electrode has a thickness of from about 290 to 310Å; the planarized first ILD layer has a thickness of about 1800Å; and the metal gate portion has a thickness of from about 1900 to 2100Å.

41. The method of claim 31, wherein the gate electrode has a height of from about 1500 to 2200Å; the silicide portion over the gate electrode has a thickness of about 300Å; the planarized first ILD layer has a thickness of about 1800Å; and the metal gate portion has a thickness of about 2000Å.

42. The method of claim 31, wherein the MOSFET includes a source silicide portion over at least a portion of the source and a drain silicide portion over at least a portion of the drain; and wherein the second metal contact contacts the drain silicide portion.

43. The method of claim 31, wherein the MOSFET includes a source $CoSi_x$ silicide portion over at least a portion of the source and a drain $CoSi_x$ silicide portion over at least a portion of the drain; and wherein the second metal contact contacts the drain $CoSi_x$ silicide portion.

44. The method of claim 31, wherein the first ILD layer is planarized by a chemical-mechanical polishing process.

45. The method of claim 31, wherein the high $f_{MAX}$ deep submicron MOSFET is used in an RF circuit.